REMARKS

Rejections under 35 U.S.C. 102

Claims 1 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,210,437 to Sawada. Applicants respectfully disagree.

Claim 1

The Examine opines that Sawada discloses (see, for example, Fig. 2E) a semiconductor device (camouflaged circuit structure) having a gate electrode (gate region) 27, substrate 21, source and drain diffusion layers (first active region/second active region) 28, and well (first well) 25. The Examiner further opines that in claim 2, Sawada discloses that the well has the same conductivity type (first conductivity type) as that of the source and drain layers. The Applicants respectfully disagree.

Generally, Sawada relates to MOS transistors wherein the threshold voltage is tuned by controlling the dimensions of the mask that is used for diffusion-doping the gate region. Sawada teaches in particular that, for a depletion MOS, using a mask opening equal to, or smaller than, two times the impurity diffusion depth results in a smaller surface impurity concentration in the gate region (and thus in a smaller threshold voltage). See for example Fig. 3B, which shows that for a mask dimension (resist space) smaller than 6um, decreasing the mask dimension decreases the surface impurity concentration (which decreases the threshold voltage).

Sawada teaches (col. 3, lines 63-65) that for the minimum (null) mask dimensions, the impurity doping concentration falls to the doping level of the P-substrate. Applicants note that with such a doping level however, there is no electrical path between the source and drain and the transistor cannot operate as a depletion transistor.

Sawada also teaches (e.g. see Fig. 3B) that increasing the dimensions of the mask (above two times the impurity diffusion depth) leads to a rapid leveling of the impurity concentration (i.e. 5.10^{17} cm^{-3} in Fig. 3B). Applicants note that this maximum impurity concentration is in particular the impurity concentration obtained with a "regular" mask (larger than two times the impurity diffusion depth) when manufacturing a "regular" depletion transistor.

The threshold voltage depending from the impurity concentration, Sawada's invention allows controlling the threshold voltage of a depletion transistor between a minimum value (for a mask having small but non-null dimensions) and a maximum value (for a mask larger than two times the impurity diffusion depth) corresponding to the threshold voltage of a regular depletion transistor.

Applicants note that Sawada does not disclose or suggest that a regular depletion transistor may have a threshold voltage higher than a "reasonable" voltage as recited in claim 1 (and defined in the application as referring to any gate voltage found in normal device operation such that the voltage does not break down the gate oxide). Accordingly, Sawada only teaches a circuit wherein the well 25 provides an electrical path between the source and drain until a threshold voltage (smaller than, or equal to, a regular threshold voltage) is applied to the circuit.

In view of the above, Applicants respectfully submit that claim 1 is patentable over Sawada, at least because the Examiner has failed to show that Sawada discloses or suggests a circuit as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*.

Claim 5

We respectfully submit that at least in view of its dependency on claim 1, claim 5 is patentable over Sawada.

Rejections under 35 U.S.C. 103

Claims 2, 3 and 4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada in view of U.S. Pat. No. 3,938,620 to Spadea, and claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. 4,860,084 to Shibata in view of U.S. Pat. No. 4,145,701 to Kawagoe. Applicants respectfully disagree.

Claims 2, 3 and 4

Claims 2, 3 and 4 depend directly or indirectly on claim 1. Applicants note that the Examiner has failed to show that Spadea shows a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*. In view of the above, Applicants submit that the Examiner has failed to show that Sawada or Spadea, alone or in combination, would have led one of ordinary skill to a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*. Accordingly, Applicants respectfully submit that claim 1 is patentable over Sawada in view of Spadea, and respectfully submit that at least in view of their dependency on claim 1, claims 2, 3 and 4 are patentable over Sawada in view of Spadea.

Claim 6

Shibata relates to semiconductor devices in which fine contact portions to connect elements with conductive wires are formed (col. 1, lines 10-12). In particular, Shibata discloses (Fig. 4) an enhancement MOS having two "wells" (76, 78) of a conductivity type different from the source & drain regions (12, 14), which are disposed under the source & drain regions and that are separated from the gate region (under Q1). Applicants note that these two underlying "wells" (76, 78) are used to *"prevent the occurrence of 'punch through' which result in a leakage current flowing between the V-shaped contact concave portions 22 and 72"* (col. 6, lines 38-46), wherein the *"contact concave portions"* 22 and 72 are in contact with metal wiring layers 80 and 84 through holes 20 and 70.

Kawagoe discloses a circuit comprising a plurality of insulated gate field effect enhancement transistors, wherein a high degree of integration is achieved by generally replacing connections using aluminum wiring (and contact holes) by depletion transistors (col. 3, lines 42-48 and 55-58).

Accordingly, Applicants respectfully submit that one skilled in the art would have lacked motivation to combine Shibata, which relates to an improvement of the contact portions to connect elements with conductive wires, and Kawagoe, which relates to suppressing such contact portions (col. 3, lines 55-58).

Applicants also note that the two underlying "wells" (76, 78) of Shibata are provided to prevent leakage current to flow between the contact portions, whereas the structure of Kawagoe provides for improving the density of integration by suppressing such contact portions. Accordingly, even if one skilled in the art had, for an undisclosed reason, decided to combine the teachings of Shibata and Kawagoe, the arrangement of Kawagoe would have led to suppressing the contact portions of Shibata, which would have suppressed at the same time the underlying "wells" (76, 78) of Shibata.

In view of the above, the Applicants respectfully submit that the Examiner has failed to show that one skilled in the art would have been motivated to combine the teachings of Shibata and Kawagoe. Besides, even if one skilled in the art had combined these teachings, one wouldn't have obtained a circuit as recited in claim 6, and in particular comprising *"a plurality of wells of a second conductivity type being partially disposed under said at least two of said plurality of active regions"*. At least in view of the above, claim 6 is patentable over Shibata in view of Kawagoe.

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In view of all of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendments, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

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